We Claim:

1. A contact configuration, comprising:

a semiconductor body of semiconductor material in a monocrystalline phase;

a metalization layer; and

a layer of said semiconductor material in a substantially amorphous phase disposed between said semiconductor body and said metalization layer, for forming an ohmic contact between said metalization layer and said semiconductor body.

2. The contact configuration according to claim 1, wherein said semiconductor material is silicon.

3. The contact configuration according to claim 2, wherein said layer is a layer of amorphous silicon doped with hydrogen.

4. The contact configuration according to claim 2, wherein said layer is a layer of amorphous silicon with oxygen atoms incorporated therein.

5. The contact configuration according to claim 2, wherein said silicon semiconductor body is n-conducting in a region of said layer of amorphous silicon.

6. The contact configuration according to claim 2, wherein said layer is a layer of amorphous silicon additionally doped with phosphorus.

7. The contact configuration according to claim 2, wherein said layer is a layer of amorphous silicon doped with boron.

8. The contact configuration according to claim 2, wherein said silicon semiconductor body is p-conducting in a region of said layer of amorphous silicon.

9. The contact configuration according to claim 1, wherein said layer of amorphous semiconductor material has a thickness in the order of magnitude of nanometers.

10. The contact configuration according to claim 9, wherein said thickness of said layer lies between 2 and 100 nm.

11. The contact configuration according to claim 1, wherein said layer of amorphous semiconductor material has a doping of between 10^{15} and 10^{16} charge carriers per cm^3.

12. The contact configuration according to claim 1, wherein said metalization layer is formed of a metal selected from the group consisting of aluminum, chromium, and aluminum/ chromium.

13. The contact configuration according to claim 1, which comprises one of a trench component and a planar component formed in said semiconductor body.

14. The contact configuration according to claim 13, wherein said component is selected from the group consisting of a diode, a bipolar transistor, a MOSFET, and an IGBT.

15. The contact configuration according to claim 1, which comprises a field stop zone in said semiconductor body, said field stop zone adjoining said layer of said amorphous semiconductor material.

16. The contact configuration according to claim 1, which further comprises an additional layer in said semiconductor body in a region of said layer of amorphous semiconductor material, said additional layer forming an emitter.

17. The contact configuration according to claim 16, wherein said additional layer and said semiconductor body are of a common conductivity type.

18. The contact configuration according to claim 16, wherein said additional layer and said semiconductor body having mutually opposite conductivity types.

19. The contact configuration according to claim 16, wherein said additional layer is doped so weakly that, without said layer of amorphous semiconductor material, said additional layer forms one of a Schottky contact or an ohmic contact with a relatively high contact resistance.

20. The contact configuration according to claim 1, wherein said layer of amorphous semiconductor material is formed on at least one of a front side and a rear side of said semiconductor body.

21. The contact configuration according to claim 20, wherein said layer of amorphous semiconductor material is formed to locally attenuate an injection of charge carriers in critical component regions.

22. The contact configuration according to claim 1, wherein said layer of amorphous semiconductor material is locally recrystallized.

23. The contact configuration according to claim 1, wherein in said amorphous semiconductor material is silicon carbide.

24. A method for producing the contact configuration according to claim 1 which comprises:

providing a semiconductor body;

applying amorphous semiconductor material on the semiconductor body by a process selected from the group consisting of sputtering, vapor deposition, and glow discharge; and

subsequently subjecting the amorphous semiconductor material to heat treatment and forming the contact configuration according to claim 1.

25. The method according to claim 24, which comprises performing the heat treatment at about 350°C to 450°C.

26. The method according to claim 24, which comprises sputtering in a hydrogen-containing atmosphere.

27. The method according to claim 24, which comprises performing the heat treatment in a hydrogen-containing atmosphere.

28. The method according to claim 24, which comprises locally recrystallizing the amorphous layer of silicon at temperatures above about 600°C in component regions.

29. A method for producing the contact configuration according to claim 1 which comprises:

providing a semiconductor body; and

forming an amorphous semiconductor material in the semiconductor body by damage formation, and producing the contact configuration according to claim 1.

30. The method according to claim 29, which comprises doping the amorphous semiconductor material.

31. The method according to claim 29, wherein the amorphous semiconductor material is doped with a material selected from the group consisting of boron and phosphorous.

32. The method according to claim 29, which comprises introducing an additional layer into the semiconductor body in a region of a layer formed of amorphous semiconductor material.

33. The method according to claim 32, wherein the additional layer is weakly doped.

34. The method according to claim 29, wherein the damage formation is effected by implantation.

35. The method according to claim 34, wherein the implantation comprises implanting elements of the third period of the periodic table of elements.

36. The method according to claim 34, which comprises implanting with an implantation dose of about $5 \cdot 10^{14}$ cm^{-2} to $1 \cdot 10^{16}$ cm^{-2}.

37. The method according to claim 29, which comprises locally recrystallizing the amorphous layer of silicon at temperatures above about 600°C in component regions.